Synchronous Buck Converter
With Power Good Detector and LDO

General Description
The iD8240 is optimized for high-performance microprocessor applications consisting of a synchronous step-down DC/DC converter and a high-speed LDO regulator. A power good detector and a LDO enable control are also built-in. The DC/DC converter operates on a current-mode architecture for excellent line and load transient responses. The operation frequency is 1MHz, allowing the use of a small surface mount inductor as well as a small capacitor. The internal synchronous switch increases efficiency and requires no external schottky diode. The iD8240 is one of our synchronous step-down DC/DC converter series that is ideally suitable for systems powered form a 1-cell Li-ion battery or from a 3-cell to 4-cell NiCd, NiMH, or alkal or alkaline battery. It also fits well in USB-based power system.

Ordering Information
iD8240 - □□□□□□
Package F3A:DFN-10

DC/DC Voltage Voltage Code
1.2 12
1.8 18
2.5 25

Applications
- Portable Instrument
- Graphic Cards
- DSC
- PDAs

Features
- Operation Voltage 2.5V~6.0V
- Oscillation frequency 1MHz
- Output Current Maximum 400mA (DC-DC Converter)
- Built-In 400mA/LDO
- Power Good Indicator with Time Delay Adjustable
- Built-In Current Limit
- Built-In UVLO
- Built-In Thermal ShutDown
- RoHS / Green Compliant

Marking Information
For marking information, please contact our sales representative directly or through distributor around your location.
Typical Application Circuit

Absolute Maximum Ratings
- Supply Voltage VIN: 6V
- Power Dissipation, PD @ TA=25°C: 400mW
- Thermal Resistance, Θja: 250°C/W
- Lead Temperature: 260°C
- Storage Temperature: -65°C to 150°C

Recommended Operating Conditions
- Input Voltage VIN: 2.2V to 6V
- EN Input Voltage: 0V to 6V
- Junction Temperature: -40°C to 125°C
- Ambient Operating Temperature: -40°C to 85°C
Pin Configurations

(Top View)

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PG</td>
<td>Power Good Indicator Output (Active High)</td>
</tr>
<tr>
<td>2</td>
<td>OUT1</td>
<td>DC/DC Output (1.8V or 1.2V)</td>
</tr>
<tr>
<td>3</td>
<td>VCC</td>
<td>Power Supply</td>
</tr>
<tr>
<td>4</td>
<td>SW</td>
<td>DC/DC Inductor Node</td>
</tr>
<tr>
<td>5</td>
<td>PGND</td>
<td>Power Ground</td>
</tr>
<tr>
<td>6</td>
<td>VBG</td>
<td>Reference Output Voltage</td>
</tr>
<tr>
<td>7</td>
<td>AGND</td>
<td>Analog Ground</td>
</tr>
<tr>
<td>8</td>
<td>DELAY</td>
<td>The capacitor connection terminal for LDO control and PG delay time setup</td>
</tr>
<tr>
<td>9</td>
<td>OUT2</td>
<td>LDO Output (3.3V)</td>
</tr>
<tr>
<td>10</td>
<td>BPC</td>
<td>LDO Input By-pass Capacitor Node</td>
</tr>
<tr>
<td>Bottom</td>
<td>GND</td>
<td>Analog Ground</td>
</tr>
</tbody>
</table>
Function Block Diagram
## Electrical Characteristics (VCC = 3.6V, Ta = +25°C, unless otherwise noted.)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DC/DC CONVERTER</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC UVLO</td>
<td>$V_{UV}$</td>
<td>$V_{CC}$ = 3V to 2V Sweep</td>
<td>- 2.4 - -</td>
<td>V</td>
</tr>
<tr>
<td>UVLO Hysteresis width</td>
<td>$V_{UVHY}$</td>
<td>- 100 - -</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Input Supply Range</td>
<td>$V_{CC}$</td>
<td>2.5 - 6.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>$I_S$</td>
<td>Active Mode</td>
<td>- 120 - -</td>
<td>µA</td>
</tr>
<tr>
<td>Output1 Voltage Accuracy</td>
<td>$V_{OUT1}$</td>
<td>- - +3</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Output1 Voltage line-regulation</td>
<td>$V_{OUT1_LINE}$</td>
<td>$V_{CC}$ = 3.5V to 6.0V</td>
<td>- 0.1 0.5 - -</td>
<td>%</td>
</tr>
<tr>
<td>Output1 Variation with Temperature</td>
<td>$I_{CL1}$</td>
<td>$V_{IN}$ = 5V, $V_{OUT1}$ = 2.5V/1.8V</td>
<td>1.3 - - - -</td>
<td>A</td>
</tr>
<tr>
<td>Maximum Output Current</td>
<td>$I_O$</td>
<td>$V_{IN}$ = 5V, $V_{OUT1}$ = 2.5V/1.8V, $L$ = 4.7uH</td>
<td>400 - - - -</td>
<td>mA</td>
</tr>
<tr>
<td>Oscillator Frequency</td>
<td>$f_{osc1}$</td>
<td>$V_{OUT1}$ = 2.5V/1.8V</td>
<td>0.8 1.0 1.2 -</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>$f_{osc2}$</td>
<td>$V_{OUT1}$ = 0V</td>
<td>- 200 - -</td>
<td>KHz</td>
</tr>
<tr>
<td>RDS(ON) of P-Channel MOSFET</td>
<td>$R_{PFET}$</td>
<td>$I_{LX}$ = 300mA</td>
<td>- 0.3 0.4 - -</td>
<td>Ω</td>
</tr>
<tr>
<td>RDS(ON) of N-Channel MOSFET</td>
<td>$R_{NFET}$</td>
<td>$I_{LX}$ = -300mA</td>
<td>- 0.25 0.35 - -</td>
<td>Ω</td>
</tr>
<tr>
<td>SW Leakage Current</td>
<td>$I_{SWL}$</td>
<td>- ±0.1 ±1 - -</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td><strong>CONTROL BLOCK</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PG on voltage</td>
<td>$V_{PGON}$</td>
<td>$I_{PG}$ = 1mA</td>
<td>- - 0.4 - -</td>
<td>V</td>
</tr>
<tr>
<td>PG Hysteresis width</td>
<td>$V_{PGHY}$</td>
<td>- 80 - -</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>PG pin leak current</td>
<td>$I_{PGTLK}$</td>
<td>$V_{PG}$ = 5.0V</td>
<td>- - 1 - -</td>
<td>uA</td>
</tr>
<tr>
<td>LDO control on Hysteresis width</td>
<td>$V_{LDTHYS}$</td>
<td>- 80 - -</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>DELAY Pin Charge Current</td>
<td>$I_{DELAY}$</td>
<td>0.8 1.0 1.2 -</td>
<td>uA</td>
<td></td>
</tr>
<tr>
<td><strong>LDO</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output2 Voltage Accuracy</td>
<td>$V_{OUT2}$</td>
<td>- - +2 - -</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Current Limit</td>
<td>$I_{CL2}$</td>
<td>450 - -</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_{DV}$</td>
<td>$I_{OUT2}$ = 400mA</td>
<td>- 600 - -</td>
<td>V</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>$\Delta V_{OUT2}$</td>
<td>$I_{OUT2}$ = 1mA -&gt; 100mA</td>
<td>- 15 50 - -</td>
<td>mV</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>LR</td>
<td>$I_{OUT2}$ = 100mA, $V_{CC}$ = 3.6V to 6.0V</td>
<td>0.05 0.25 - -</td>
<td>%</td>
</tr>
<tr>
<td>Ripple Rejection Rate</td>
<td>PSRR</td>
<td>$I_{OUT2}$ = 100mA, $f$ = 1kHz</td>
<td>- 60 - -</td>
<td>dB</td>
</tr>
<tr>
<td>OUT2 Leakage Current</td>
<td>$I_{OUT2LK}$</td>
<td>- - 6 - -</td>
<td>uA</td>
<td></td>
</tr>
</tbody>
</table>
Typical Operating Characteristics

**Quiescent Current vs. Supply Voltage**

- **Supply Voltage (V)**
  - 3.5 to 6 V
  - Quiescent Current (uA)
    - 80 to 140 uA

**Dropout Voltage vs. Output Current**

- **Output Current (A)**
  - 50 to 400 mA
  - Dropout Voltage (V)
    - 0.00 to 0.250 V

**Input Voltage vs. Output Voltage**

- **Input Voltage (V)**
  - 2.5 to 6 V
  - Output Voltage (V)
    - 1.5 to 1.25 V
- **I_{LOAD}=50mA**

**Input Voltage vs. Output Voltage**

- **Input Voltage (V)**
  - 3.5 to 6 V
  - Output Voltage (V)
    - 3.0 to 3.5 V
- **I_{LOAD}=50mA**

**Output Voltage vs. Output Current**

- **Output Current (mA)**
  - 0 to 400 mA
  - Output Voltage (V)
    - 1.5 to 1.275 V
- **V_{IN} = 5V**

**Output Voltage vs. Output Current**

- **Output Current (mA)**
  - 0 to 400 mA
  - Output Voltage (V)
    - 3.0 to 3.5 V
- **V_{IN} = 5V**
**Efficiency vs. Output Current**

- Efficiency (%) vs. Output current (mA)
- Output current: 5V
- Output voltage: 1.8V, 1.2V

**R\text{ON} vs. Supply Voltage**

- Supply Voltage (V) vs. R\text{ON} (\text{m}\Omega)
- LX\text{CURRENT} = 300mA

**Current Limiting vs. Supply Voltage**

- Supply Voltage (V) vs. Current Limiting (A)
- V\text{OUT1} connect 0.5\Omega to GND
- V\text{OUT2} connect 0.5\Omega to GND

**Frequency vs. Supply Voltage**

- Frequency (KHz) vs. Supply Voltage (V)
- I\text{LOAD1} = 300mA
Light Load Operation

\[ V_{\text{IN}} = 5V, \ I_{\text{LOAD}} = 50 \text{mA} \]

Heavy Load Operation

\[ V_{\text{IN}} = 5V, \ I_{\text{LOAD}} = 400 \text{mA} \]

Load Transient Response

\[ V_{\text{IN}} = 5V, \ I_{\text{LOAD1}} = 0.1 \text{ to } 0.3A, \ I_{\text{LOAD2}} = 0.2A \]

Line Transient Response

\[ V_{\text{IN}} = 4 \text{ to } 5V, \ I_{\text{LOAD}} = 10mA \]
Startup from Shutdown

\[ V_{IN} = 5V \]

\[ V_{IN-DC} \ (5V/Div) \]

\[ V_{OUT1-DC} \ (1V/Div) \]

\[ V_{OUT2-DC} \ (2V/Div) \]

\[ PG_{DC} \ (2V/Div) \]

Time (5ms/Div)

Startup from Shutdown

\[ V_{IN} = 5V \]

\[ Delay_{DC} \ (1V/Div) \]

\[ V_{OUT1-DC} \ (2V/Div) \]

\[ V_{OUT2-DC} \ (5V/Div) \]

\[ PG_{DC} \ (2V/Div) \]

Time (5ms/Div)

PG Detector with Current Limit

\[ V_{IN} = 5V, V_{OUT1} \text{ connect } 0.5\Ohm \text{ to GND} \]

\[ V_{IN-DC} \ (5V/Div) \]

\[ V_{OUT1-DC} \ (1V/Div) \]

\[ V_{OUT2-DC} \ (2V/Div) \]

\[ PG_{DC} \ (2V/Div) \]

Time (250us/Div)

PG Detector with Current Limit

\[ V_{IN} = 5V, V_{OUT2} \text{ connect } 0.5\Ohm \text{ to GND} \]

\[ V_{IN-DC} \ (5V/Div) \]

\[ V_{OUT1-DC} \ (2V/Div) \]

\[ V_{OUT2-DC} \ (2V/Div) \]

\[ PG_{DC} \ (1V/Div) \]

Time (100us/Div)

VBG Startup Response Time

\[ V_{IN} = 5V \]

\[ V_{IN-DC} \ (5V/Div) \]

\[ V_{OUT1-DC} \ (2V/Div) \]

\[ V_{OUT2-DC} \ (2V/Div) \]

\[ VBG_{DC} \ (2V/Div) \]

Time (5ms/Div)
Application Information

In continuous mode, the source current of the top MOSFET is square wave of duty cycle. The primary function of the input capacitor is to provide a low impedance loop for the edges of pulsed current drawn by the iD8240. A load step at the output can induce ringing at the input VIN. This ringing can couple to the output and be mistaken as loop instability. The oscillation can be improved by add the capacitance of the input capacitor. A typical value is 10 μF ceramic (X5R or X7R), POSCAP or Aluminum Polymer. These capacitors will provide good high frequency bypassing and their low ESR will reduce resistive losses for higher efficiency. The input capacitor RMS current varies with the input voltage and the output voltage. The equation for the maximum RMS current in the input capacitor is:

$$I_{RMS} = I_{MAX} \frac{V_o}{V_{IN}} \left(1 - \frac{V_o}{V_{IN}}\right)$$

The output capacitor depends on the suitable ripple voltage. Low ripple voltage corresponds to lower effective series resistance (ESR). The output ripple voltage is determined by:

$$\Delta V_{OUT} = \Delta L \left(ESR + \frac{1}{8 f_{OUT}}\right)$$

The output capacitor RMS ripple current is given by:

$$I_{RMS} = \frac{1}{2\sqrt{3}} \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times f \times V_{IN}}$$

VBG Capacitor

A VBG pin is provided to decouple the bandgap reference voltage. An external capacitor connected form VBG to GND reduces noise present on the internal reference voltage, which in turn significantly reduces output noise and also improves PSRR. Larger capacitor values may be used to further improve PSRR, but result in a longer time period (slower turn on) to settle output voltage when power is initially applied.

LDO

For general purposes, use a 2.2μF capacitor on the LDO output. Larger capacitor values and lower ESR provide better supply noise rejection and transient response. A higher value input capacitor may be necessary if large, fast transients are anticipated. Ceramic capacitors have the lowest ESR, and will offer the best AC performance.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Inductor Selection

The inductor is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple current. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor. The inductor is selected to limit the ripple current to some predetermined value, typically 20~40% of the full load current at the maximum input voltage. The formula of inductance value is as below:

$$\Delta L = 0.2 \sim 0.4 \times I_{OUT(MAX)}$$

$$L = \frac{V_{OUT}}{f \times \Delta L} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$I_{pk} = I_0 + \frac{\Delta L}{2} = I_0 + \frac{(V_{IN} - V_{OUT}) \times I_{OUT}}{2 \times L}$$

Power Good Indicator with Adjustable Time Delay

When OUT1 pin is above 2.25V or 1.62V (typ.) and with a delay time (t1) the OUT2 is start to regulation.
The PG pin terminal is an open drain output of N-MOS. Connect a resistor from PG pin to VCC or OUT2 to create a logic signal. If OUT2 pin is less than 2.97V (typ.) this pin is pulled to ground. When OUT2 pin is above 2.97V (typ.) and with a delay time (t2) this pin is open. PG pin is forced low when in UVLO.

The formula of adjustable delay time is as below:

\[ \text{delay-time} = t1 = t2 = C \times \frac{0.7V}{I_{\text{delay}}} \]

**The Dissipation**

The power loss is given by:

\[ P_{\text{LOSS}(\text{DC-DC})} = I_{\text{OUT}}^2 \times R_{\text{BS(on)}} - I_{\text{OUT}} \times D + I_{\text{OUT}}^2 \times R_{\text{BS(on)}} - I_{\text{OUT}} \times (1 - D) + \frac{1}{2} \times V_{\text{IN}} \times I_{\text{OUT}} \times (t + t2) \times f_s + \frac{1}{2} \times V_{\text{IN}} \times I_{\text{OUT}} \times (t + t2) \times f_s + L \times V_{\text{IN}} \]

\[ P_{\text{LOSS(LDO)}} = I_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}}) \]

\[ T_{\text{JMAX}} = T_\alpha + \theta_\alpha \times (P_{\text{LOSS(DC-DC)}} + P_{\text{LOSS(LDO)}}) \]

**Recommended component selection for Typical Application**

**Table 1. Inductors**

<table>
<thead>
<tr>
<th>Component Supplier</th>
<th>Series</th>
<th>Inductance (uH)</th>
<th>DCR (mΩ)</th>
<th>Rated Current (A)</th>
<th>Dimensions (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sumida</td>
<td>CDRH4D283R3</td>
<td>3.3uH</td>
<td>36.4</td>
<td>1.57</td>
<td>5X5X3</td>
</tr>
<tr>
<td>Sumida</td>
<td>CDRH4D284R7</td>
<td>4.7uH</td>
<td>53.3</td>
<td>1.32</td>
<td>5X5X3</td>
</tr>
<tr>
<td>Wurth Elektronik</td>
<td>744043003</td>
<td>3.3uH</td>
<td>30</td>
<td>2.1</td>
<td>4.8X4.8X2.8</td>
</tr>
<tr>
<td>Wurth Elektronik</td>
<td>744043004</td>
<td>4.7uH</td>
<td>52</td>
<td>1.55</td>
<td>4.8X4.8X2.8</td>
</tr>
</tbody>
</table>

**Table 2. Capacitors for Cin and Cout**

<table>
<thead>
<tr>
<th>Component Supplier</th>
<th>Series</th>
<th>Capacitance (uF)</th>
<th>Case Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDK</td>
<td>C2012X5R0J106M</td>
<td>10</td>
<td>0805</td>
</tr>
<tr>
<td>Panasonic</td>
<td>ECJ4YB1A106M</td>
<td>10</td>
<td>1210</td>
</tr>
<tr>
<td>TAIYO YUDEN</td>
<td>JMK212BJ106ML</td>
<td>10</td>
<td>0805</td>
</tr>
</tbody>
</table>
Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the iD8240. These items are also illustrated graphically in layout diagram. Check the following in your layout:

1. The power traces, consisting of the GND trace, the SW trace and the VIN trace should be kept short, direct and wide.

2. Does the OUT1 pin connect directly to the V_{OUT1}?
The OUT1 pin must be connected between the (+) plate of C_{OUT1}.

3. Does the (+) plate of C_{IN} connect to V_{IN} as closely as possible?
This capacitor provides the AC current to the internal power MOSFETs.

4. Keep the switching node, SW, away from the sensitive OUT1 node.

5. Keep the (–) plates of C_{IN} and C_{OUT1} and C_{OUT2} as close as possible.

6. Keep C_{BG} must be near VBG pin, this pin can affect the LDO regulator output noise and voltage regulation performance.

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Layout Diagram

Top over Layer

Top Layer

Bottom Layer
Packaging

DFN-10

<table>
<thead>
<tr>
<th>SYMBOLS</th>
<th>DIMENSIONS IN MILLIMETERS</th>
<th>DIMENSIONS IN INCH</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
<td>NOM</td>
</tr>
<tr>
<td>A</td>
<td>0.80</td>
<td>0.90</td>
</tr>
<tr>
<td>A1</td>
<td>0.00</td>
<td>0.01</td>
</tr>
<tr>
<td>A3</td>
<td>---</td>
<td>0.2 REF</td>
</tr>
<tr>
<td>b</td>
<td>0.18</td>
<td>0.23</td>
</tr>
<tr>
<td>D</td>
<td>2.95</td>
<td>3.0 BSC</td>
</tr>
<tr>
<td>D1</td>
<td>---</td>
<td>2.2 BSC</td>
</tr>
<tr>
<td>E</td>
<td>2.85</td>
<td>3.0 BSC</td>
</tr>
<tr>
<td>E1</td>
<td>---</td>
<td>1.6 BSC</td>
</tr>
<tr>
<td>e</td>
<td>---</td>
<td>0.5BSC</td>
</tr>
<tr>
<td>L</td>
<td>0.30</td>
<td>0.40</td>
</tr>
<tr>
<td>θ</td>
<td>-12°</td>
<td>---</td>
</tr>
</tbody>
</table>